

Application No.:09/539,966  
Response dated October 16, 2003  
Reply to Office Action of June 18, 2003

### **REMARKS/ARGUMENTS**

The above-identified patent application has been amended and reconsideration and re-examination are hereby requested.

With regard to the provisional double patenting rejection, it is respectfully noted that this is a provisional rejection and will be addressed when claims in this application have been allowed since only then can the issue be considered by the applicant.

The claims stand rejected under 35 USC 102(b) as being anticipated by Martin et al., U. S. Patent No. 5,214,768.

The Examiner takes the position that it is inherent to combine the first directors into a plurality of director boards. It is respectfully submitted that this is not inherent.

Before discussing the claims and how they distinguish over the cited art, perhaps it might be helpful to review features of Applicant's invention.

Referring to FIG. 2 of the patent application, data passes between the host computer and disk drives through the global cache memory 220 with messages passing between the directors through the message network 260. Thus, the messages do not pass through the global cache memory, whereas the data does pass through the global cache memory.

Referring to FIG. 5 of the patent application, the message network 260 includes a pair of cross bar switches 308. There are a plurality of front end directors on printed circuit boards 190 each connected to a cross bar switch 320. There are also a plurality of back end directors on printed circuit boards 190 each connected to a cross bar switch 320. The cross bar switches 320 are connected to the cross bar switches 308 of the message network 160..

More particularly, it is noted that each crossbar switch 320 has a pair of ports 325<sub>1</sub> AND 325<sub>2</sub>. Further, it is noted that there are TWO crossbar switches 308 in the message network 160.

Claim 1-15 and new claim 30 point out that each one of the boards has a PAIR of "output/input ports" and that the message network is coupled to the pair of output/input ports

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of the director boards. Such is not INHERENT in Martin et al.

**Further, such is not obvious over the claims in patent application serial no. 09/540,828.**

Applicant respectfully requests that the Examiner point out:

- (1) which element in Martin et al. does the Examiner consider the cache memory; and
- (2) which element in Martin et al. does the Examiner consider the cache memory; and
- (3) where is there a data transfer between first directors and the second directors **with such data passing through the cache memory in response to messages passing between the first directors and the second directors through the messaging network.**

#### **REQUEST FOR TELEPHONE INTERVIEW**

**If, after reviewing this response, the Examiner still maintains a rejection of the claims, applicant's attorney hereby requests a telephone interview with the Examiner in order to discuss any issues prior to issuing any office action. The Applicant's attorney can be reached at either the number listed below or at 508 4877 4311.**

#### **Referring now to the independent claims:**

Claim 1-14 also point out that:

such cache memory being coupled to the plurality of first and second directors;

...

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a message network, operative independently of the data transfer section, coupled to the pair of output/input ports of each one of the directors boards of the plurality of first director boards and to the pair of output/input ports of each one of the directors boards of the plurality of second director boards; and

wherein the first and second directors control data transfer between the first directors and the second directors in response to messages passing between the first directors and the second directors through the message network to facilitate data transfer between first directors and the second directors with such data passing through the cache memory in the data transfer section.

Applicant respectfully requests that the Examiner point out where in Martin:

(1) there is the cache memory coupled to the plurality of first and second directors;

(2) there is a message network operative independently of the data transfer section; and

(3) the first and second directors control data transfer between the first directors and the second directors in response to messages passing between the first directors and the second directors through the message network to facilitate data transfer between first directors and the second directors with such data passing through the cache memory in the data transfer section.

Similar limitations are in claims 15- 28 and Applicant, with regard to such claims, makes the same request of the Examiner.

New claim 29 points out that: " such messages by-passing the data transfer section and with such data transfer comprising passing data through the directors to the cache memory in the data transfer section" (emphasis added).


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New claim 31 points out that each one of the messages includes a destination field.

In the event any additional fee is required, please charge such amount to Patent and Trademark Office Deposit Account No. 50-0845.

Respectfully submitted,

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Date

  
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